CLAIMS

1. A method of forming a conductor wiring pattern, comprising the following steps of:

forming a first insulating layer on a surface of a substrate and also forming a second, photosensitive insulating resin layer thereon;

light-exposing and developing the second insulating layer to form pattern grooves so that the first insulating layer is exposed at bottoms of the pattern grooves;

forming a plating seed layer on the second insulating layer including inner surfaces of the pattern grooves and then forming a resist pattern on the plating seed layer except for portions of the pattern grooves;

filling the pattern grooves with a conductor by an electrolytic plating using the plating seed layer as a power supply layer; and

removing the resist pattern and also removing the seed layer exposed on the surface of the second insulating layer to form wiring pattern consisting of conductors remained in the pattern grooves.

2. A method as set forth in claim 1, wherein a plurality of different metal layers are used, as the conductor, when the pattern grooves are filled with the conductor by the electrolytic plating.

3. A method as set forth in claim 2, wherein the plurality of different metal layers are at least two metal layers consisting of a copper base layer and a nickel barrier layer.

4. A method as set forth in claim 1, wherein the first insulating layer is composed of a photosensitive insulating resin;

after the first insulating layer is light-exposed and developed to form an opening, through which a first wiring pattern formed on the substrate is to be electrically connected to a second wiring pattern to be formed on the first insulating layer, the first

insulating layer is heated and hardened.

5. A method as set forth in claim 1, wherein a semiconductor wafer is used as the substrate, the semiconductor wafer has an electrode terminal forming surface, on which the first insulating layer and the second insulating layer are formed, and the wiring pattern, which is electrically connected with electrode terminals of the semiconductor wafer, is formed.